PCT #4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: BURNS, Geoffrey Docket No.: US02 0543 US

PTO Application No.: 10/538369 Conf.: Unknown Art Unit: Unknown

Date Filed: 06/10/2005 Examiner: Unknown

Title: Modular Integration of an Array Processor within a System on Chip

Mail Stop DD
Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

TRANSMITTAL OF
INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97

Sir:

Enclosed in this transmittal is an "Information Disclosure Statement by Applicant" and a copy of each of the documents listed thereon. These documents are considered to be relevant in that they have been cited as an "X" or "Y" document in a foreign Patent Office search report on a foreign counterpart application, a copy of which report is also enclosed.

☐ I hereby certify that these documents were cited in said search report not more than three (3) months prior to the filing of this information disclosure statement.

This disclosure is not an admission that any of these documents is material to or even prior art with respect to the above-referenced application.

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees which may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

Date: 11/21/05

Respectfully submitted,

By _____

USPTO Customer Number
24738

Michael J. Ure, Reg. No. 33,089
Philips Electronics North America Corp.
1109 McKay Drive, M/S-41SJ, San Jose, CA 95131
(408) 474-9077

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" on the date indicated below.

(Date) 11/21/05 (Signature) _____
(Name) Vilimaina Naga

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Application Number	10/5[redacted]9
Filing Date	06/10/2005
First Named Inventor	BURNS, Geoffrey
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	**US02 0543 US**

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number No.-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- US 2003/0065904	04-03-2003	GEOFFREY BURNS ET AL	
	2	US- US 5 974 537	10-26-1999	VIJAY KRISHNA MEHRA	
	3	US- 60/432971		G.BURNS ET AL	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number (ctry[3]-no.[4]-kind[5], if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in capital letters), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	1	MIYAMORI T EL AL: "REMARC: RECONFIGURABLE MULTIMEDIA ARRAY COPROCESSOR ";IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS, INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG.; TOKYO, JP; Vol. E82-D, no. 2; February 1999 (1999-02); pages 389-397	
	2	CUCCHIARA R ET AL: "RECONFIGURING THE BOUNDARIES OF A MESH-CONNECTED ARRAY OF PROCESSORS . . . "; MICROPROCESSORS AND MICROSYSTEM, IPC BUSINESS PRESS LTD; LONGDON, GB; Vol. 17, no. 2; January 1993 (1993-01); pages 67-73	
	3	BARAT F ET AL INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "RECONFIGURABLE INSTRUCTION SET PROCESSORS: AN IMPLEMENTATION . . . "; CONFERENCE RECORD OF THE 35TH ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS, & COMPUTERS; PACIFIC GROOVE, CA; NOV 4-7, 2001; ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS AND COMPUTERS, NEW YORK; Vol. 1 of 2 CONF. 35; 4 NOV. 2001; pages 481-485	
	4	CALLAHAN T J ET AL: "THE GARP ARCHITECTURE AND C COMPILER"; COMPUTER, IEEE COMPUTER SOCIETY; LONG BEACH, CA, US; Vol. 33, No. 4, April 2000 (2000-04); pages 62-69	

Examiner Signature		Date Considered	

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.